AMENDMENTS TO THE DRAWINGS

Applicant submits herewith one new drawing sheet (FIG. 11) which illustrates a sectional view of an illustrative embodiment of the present invention. Adequate support for the new drawing sheet (FIG. 11) is provided by *at least* FIG. 5(c) and FIG. 10 of the original specification. Indeed, FIG. 11 is merely a combination of original FIG. 5(c) and original FIG. 10, wherein the reference numerals 203a and 203b have been employed to more clearly reference the first and second channel regions, respectively. No new matter has been added.

Attachment: One (1) New Sheet (FIG. 11)

REMARKS

I. Status of Application

By the present amendment, claim 36 has been added. Claims 14, 16 and 29-36 are all the claims currently pending in the application. Claims 14, 16 and 29-35 presently stand rejected.

II. Claim Rejections Under 35 U.S.C. 103

The Examiner was persuaded by arguments that none of the cited references teach or suggest the features of wherein an impurity doping region is disposed such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode, as recited in claim 29. However, in response to such arguments, the Examiner has set forth new grounds of rejection for claims 29, 16 and 34-35 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Prior Art as Admitted by Applicant (hereinafter "APA") in view of Japanese Patent Application No. 2003-017502A to Nakamura (hereinafter "Nakamura 1"), in view of U.S. Patent No. 5,757,050 to Adler et al. (hereinafter "Adler"), and further in view of U.S. Patent No. 6,255,180 to Smith (hereinafter "Smith"). The Examiner has also rejected claim 14 under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura 1, in view of Alder, in view of Smith, and further in view of U.S. Patent No. 6,507,069 to Zhang et al. (hereinafter "Zhang"). Claim 30 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura 1, in view of Alder, in view of Smith, and further in view of U.S. Patent No. 5,053,849 to Izawa et al. (hereinafter "Izawa"). Claims 31-32 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura 1, in view of Alder, in view of Smith, and further in view of U.S. Patent No. 6,048,795 to Numasawa et al. (hereinafter "Numasawa"). Finally, claim 6 is rejected under 35

U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura 1, in view of Alder, in view of Smith, and further in view of U.S. Patent No. 5,914,498 to Suzawa et al. (hereinafter "Suzawa"). Applicant respectfully traverses all of the pending rejections for *at least* the reasons set forth below.

With respect to the independent claim 29, the Examiner acknowledges that Nakamura 1 does not teach that the impurity doping region is disposed such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode. However, the grounds of rejection allege that it would have been obvious to avoid positioning impurity doping region 21k in Nakamura 1 directly below either of said second and third gates so as to further mitigate the short-channel effect, as evidenced by Smith, which teaches not to position the LDD regions 20 below, and directly adjacent to, gate conductors. Accordingly, the Examiner alleges that it would have been obvious to one of ordinary skill in the art to modify the teachings of APA, Nakamura 1 and Adler with those of Smith to arrive at the claimed invention. Further, the Examiner alleges that the motivation for doing so derives from the well-known adverse consequences of short-channel effects on achievable currents (*see* Smith, column 2, lines 38-40).

Without conceding to the merits of the Examiner's rejections, Applicant has amended claim 29 to recite (among other things):

> ...wherein said second active layer comprises a first channel region disposed directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity doping region disposed between said first and second channel regions such that a portion of said impurity doping

region is not directly below either said second gate electrode or said third gate electrode.

The above features would not have been obvious in view of the cited references, or any combination thereof. For example, Smith only discloses LDD areas 20 disposed at both sides of a common source/drain region shared between two transistors (*see* FIG. 1). Such a configuration is typically used in a memory cell of DRAM. That is, as taught in Smith, channel directions in two transistors are opposite to each other.

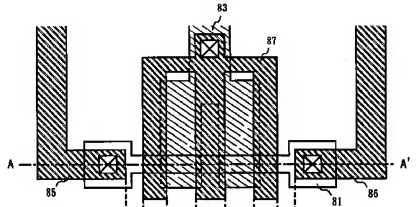
In sharp contrast to the teachings of Smith, according to illustrative embodiments of the present invention, the second gate and the third gate are included in one transistor which has one source/drain pair. That is, the channel directions in two channel regions disposed below the second gate and third gate, respectively, are the same. Therefore, Smith provides no motivation for one of ordinary skill in the art to modify the teachings of APA, Nakamura 1, and Adler to achieve the claimed invention for *at least* these reasons.

Moreover, Drawing 8 of Nakamura 1 (reproduced below) shows a double-gate structure in which an active layer comprises two channel formation fields 81a and an LDD field 81e between two channel formation fields 81a (*see* paragraphs [0083] - [0089] of the machine translation of Nakamura 1). However, as taught in Nakamura 1, the two channel formation fields 81a are disposed directly below gate electrodes 83, which according to the reasoning applied by the grounds of rejection, would allegedly correspond to the third electrode, as recited in claim 29. Further, Nakamura 1 teaches that the electrodes 87 are disposed only above LDD fields 81d, 81e and 81f. Nakamura teaches that electrodes 87 are also electrically connected to gate electrode 83

so as to have the same potential as the gate electrode 83. Moreover, the central electrode 87 overlaps the entire LDD field 81e.

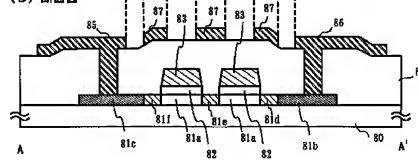
Plan View

(A) 上面図



Sectional View

(B) 断面図



Since Nakamura 1 teaches that both channel formation fields 81a are not directly below electrode 87, the electrode 87 cannot solely switch the transistor. Further, both channel regions 81a are switched simultaneously by gate electrodes 83. In such a double gate structure like that taught in Nakamura 1, the electric currents which are supplied increase as much as the number of gates is increased, and performance improves by just that amount.

However, the claimed invention is completely different than Nakamura 1. In contrast to the teachings of Nakamura 1, an illustrative embodiment of the present invention shown in FIG. 11, comprises a second gate electrode 107, which faces the first channel region 203a so that the second gate electrode can solely switch the second transistor. Consequently, as shown in FIG. 11, the TFT substrate comprises a plane configuration comprised of low voltage driven channel (second channel region) 203b, LDD 105f and high voltage driven channel (first channel region) 203a. Second gate electrode 107 is driven at higher voltage to switch the second transistor because the distance between second gate electrode 107 and first channel region 203a is longer than the distance between third gate electrode 190 and second channel region 203b. However, such a plane configuration is nowhere taught or suggested by Nakamura 1. Further, none of the cited references remedy the deficient teachings of Nakamura 1.

Therefore, claim 29 is patentable over the cited references for *at least* the above reasons. Moreover, the dependent claims 14, 16 and 30-35 are patentable *at least* by virtue of their dependency. Accordingly, Applicant respectfully requests that the Examiner withdraw these rejections.

III. New Claim

Applicant hereby adds new claim 36, which is fully supported by *at least* FIG. 10 of the original specification. No new matter has been added.

The dependent claim 36 is patentable *at least* by virtue of its dependency and by virtue of the recitations set forth therein.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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Date: November 21, 2008